

CLAIMS

- [1] (Amended) A cache memory system comprising:
a condition generation unit operable to generate a condition concerning a state of a processor;
5 a judgment unit operable to judge whether or not a current state of the processor satisfies the condition;
an address generation unit operable to generate an address to be manipulated; and
a manipulation unit operable to manipulate a cache using the
10 address generated by said address generation unit, when said judgment unit judges that the condition is satisfied,
wherein said condition generation unit is operable to generate a new condition in the case where said judgment unit judges that the condition is satisfied,.
- 15 [2] (Cancelled)
- [3] (Amended) The cache memory system according to Claim 1,
wherein said condition generation unit is operable to generate
20 a condition concerning a value of a specific register, within the processor.
- [4] The cache memory system according to Claim 3,
wherein the specific register is a program counter.
- 25 [5] (Amended) The cache memory system according to Claim 1,
wherein said condition generation unit is operable to generate, as the condition, one of memory access within a specific address range and memory access outside of the specific address range.
- 30 [6] The cache memory system according to Claim 1,
wherein said condition generation unit is operable to generate,

as the condition, execution of a specific instruction by the processor.

[7] (Amended) The cache memory system according to Claim 1,
wherein said condition generation unit is operable to generate
5 the new condition by performing a specific calculation on a current
condition.

[8] The cache memory system according to Claim 7,
wherein said condition generation unit is operable to:
10 generate a memory access address as the condition; and
generate the new condition by adding a constant to the
current condition in the case where said judgment unit judges that
the condition is satisfied.

15 [9] The cache memory system according to Claim 8,
wherein the constant is one of: an increment value or
decrement value in a post-incremented load/store instruction
executed by the processor; and a difference value of addresses in
two load/store instructions executed by the processor.

20 [10] The cache memory system according to Claim 1,
wherein said condition generation unit is operable to generate
plural conditions, and
said judgment unit is operable to judge whether or not all of
25 the plural conditions are satisfied.

[11] The cache memory system according to Claim 1,
wherein said condition generation unit is operable to generate
plural conditions, and
30 said judgment unit is operable to judge whether or not any of
the plural conditions are satisfied.

[12] (Amended) The cache memory system according to one of Claim 1 and Claim 3,

wherein said manipulation unit includes:

5 a data judgment unit operable, in the case where said judgment unit judges that the condition is satisfied, to judge whether or not data corresponding to the address generated by said address generation unit is stored in the cache;

a selection unit operable to select a line within the cache memory in the case where it is judged that the data is not stored;

10 a write back unit operable to perform a write back from the selected line when the selected line is valid and dirty;

a transfer unit operable to transfer, from a memory to the selected line after the write back, the data corresponding to the address; and

15 a registration unit operable to register the address as a tag, to the selected line.

[13] (Amended) The cache memory system according to one of Claim 1 and Claim 3,

20 wherein said manipulation unit includes:

a data judgment unit operable, in the case where said judgment unit judges that the condition is satisfied, to judge whether or not data corresponding to the address generated by said address generation unit is stored in the cache;

25 a selection unit operable to select a line within the cache memory in the case where it is judged that the data is not stored;

a write back unit operable to perform a write back from the selected line when the selected line is valid and dirty;

30 a registration unit operable to register the generated address as a tag, to the selected line, without transferring data from a memory to the selected line.

[14] (Amended) The cache memory system according to one of Claim 1 and Claim 3,

wherein said manipulation unit includes:

5 a data judgment unit operable, in the case where said judgment unit judges that the condition is satisfied, to judge whether or not data corresponding to the address generated by said address generation unit is stored in the cache;

10 a selection unit operable, in the case where it is judged that the data is stored, to select a line, within the cache memory, in which the data is stored;

a write back unit operable to perform a write back from the selected line when the selected line is valid and dirty.

15 [15] (Amended) The cache memory system according to one of Claim 1 and Claim 3,

wherein said manipulation unit includes:

20 a data judgment unit operable, in the case where said judgment unit judges that the condition is satisfied, to judge whether or not data corresponding to the address generated by said address generation unit is stored in the cache;

a selection unit operable, in the case where it is judged that the data is stored, to select a line, within the cache memory, in which the data is stored;

25 an invalidation unit operable to invalidate the selected line.

[16] (Amended) The cache memory system according to one of Claim 1 and Claim 3,

wherein said manipulation unit includes:

30 a data judgment unit operable, in the case where said judgment unit judges that the condition is satisfied, to judge whether or not data corresponding to the address generated by said address generation unit is stored in the cache;

a selection unit operable, in the case where it is judged that the data is stored, to select a line, within the cache memory, in which the data is stored;

5 a change unit operable to change an access order of the selected line in order information indicating an order in which lines are accessed.

[17] (Amended) The cache memory system according to one of Claim 12 and Claim 16,

10 wherein said condition generation unit is operable to generate a memory address as the condition, and

said manipulation unit further includes

an adjustment unit operable, in the case where the memory address generated by said condition generation unit indicates a point midway through a line, to generate an address by adjusting so
15 that one of a starting point of the line, a starting point of a next line, and a starting point of an immediately preceding line is indicated.

[18] (Amended) A cache memory control method comprising:

20 a condition generation step of generating a condition concerning a state of a processor;

a judgment step of judging whether or not a current state of the processor satisfies the condition;

25 an address generation step of generating an address to be manipulated; and

a manipulation step of manipulating a cache using the address generated in said address generation step, when it is judged in said judgment step that the condition is satisfied,

30 wherein, in said condition generation step, a new condition is generated in the case where it is judged in said judgment step that the condition is satisfied.

REPLY

5. Subject Matter of Argument:

- 5 (1) The "International Search Report and Written Opinion of the International Searching Authority (dated July 7, 2005)" concerning the present application states the opinion that Claims 1 to 4, 6, 12 and 18 lack novelty, and Claims 1 to 18 lack an inventive step.

In the present Amendment, independent Claims 1 and 18
10 have been amended to incorporate the limitations of Claim 2, Claim 2 has been cancelled, and claims dependent on the cancelled Claim 2 have been amended so as to be dependent on other claims.

Moreover, the present amendments are based on the disclosure of the Specification as filed, and do not add any new
15 matter.

Our argument as to the subject matter of the Amendment and the inclusion of an inventive step in the amended invention is as follows.

- 20 (2) Regarding amended Claim 1:

The amended Claim 1 is amended to incorporate the limitation of Claim 2. More specifically, a limitation that "said condition generation unit is operable, in the case where said judgment unit judges that the condition is satisfied, to generate a new condition" is
25 incorporated.

With this limitation, it is made clear that the condition generation unit automatically updates the condition. With this, a new condition is generated when the condition is satisfied depending on the state of the program execution by the processor. In other
30 words, the condition itself can be updated to a new condition depending on the state of the program execution by the processor, without the need for updating by software. Consequently, it is

possible to minimize software involvement and realize accurate and appropriate cache manipulation in accordance with the progress of program execution.

5 None of the cited reference documents 1 to 6 suggest the structure in which the condition itself is automatically updated. As such, we believe that, even by combining the cited reference documents 1 to 6, it is not possible to realize accurate and appropriate cache manipulation in accordance with the progress of program execution.

10 Accordingly, we believe that the structure in the amended Claim 1 cannot, even for a person of ordinary skill in the art, be easily arrived at from a combination of the cited reference documents 1 to 6, and thus includes an inventive step.

15 Furthermore, we believe that, for the same reasons, the amended Claim 18 also includes an inventive step.

(3) Regarding Claims 3 to 17:

20 Since the amended Claims 3 to 17 are dependent on amended Claim 1, we believe that they include inventive steps, for the same reasons as mentioned above.